REMARKS

After entry of this amendment, claims 1-39 are pending. In the present Office Action, claims 1-22 were rejected under 35 U.S.C. § 102(b) as being anticipated by Hinton et al., U.S. Patent No. 5,721,855 ("Hinton"). Applicant respectfully traverses this rejection and requests reconsideration.

Claims 1-27

Applicant respectfully submits that each of claims 1-22 recites a combination of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "the execution core is configured, in response to a system call instruction, to selectively update each flag of a plurality of flags responsive to a corresponding indication in the mask".

The Office Action alleges that the above highlighted features are taught by Hinton, primarily relying on Fig. 18 and the description thereof in Hinton, col. 30. Specifically, the Office Action alleges that the V field in the result buffer 1610 anticipates the plurality of flags and that the mask is anticipated by the valid bits in the RRFV field of the RAT 138. Applicant respectfully submits that there is no teaching or suggesting that the V field in the result buffer 1610 is updated responsive to the corresponding valid bits in the RRFV field. Rather, Hinton teaches "The RAT 132 also clears the RRFV bit for the EAX entry in the RAT array 1220 to indicate that the logical register EAX is mapped to the ROB 136 in a speculative state." (Hinton, col. 30, lines 45-48). That is, the RRFV bit is cleared because the real register file no longer stores the most recent (speculative) copy of the EAX register. Additionally, Hinton teaches "The ROB 136 clears the valid flag in the RE36 entry to indicate that the corresponding result data is not valid." (Hinton, col. 30, lines 65-67). That is, because the logical micro-op (the add) has not yet executed, the result data has not yet been provided.

Accordingly, the valid bit in the ROB 136 is NOT cleared responsive to the clearing of the RRFV bit in the RAT, as alleged in the present Office Action. The Office Action states "Note as shown in Fig. 18, when the mask in the RRFV field of RAT 138 at

entry EAX (ROB pointer 36) is changed from 1 to 0, then the valid bit at the corresponding entry RE36 is updated to 0 also" (See Office Action, page 3, lines 16-19). While the clearing of the RRFV bit and the clearing of the valid bit in the RE36 both occur as a result of the logically micro-op in this example, this is not sufficient to teach or suggest a selective update of each flag of a plurality of flags *responsive to* a corresponding indication in the mask.

Furthermore, Hinton teaches that, in response to the logical micro-op illustrated in Fig. 18, one valid bit is cleared in the ROB 136 (the bit in RE36). This does not teach or suggest "the execution core is configured, in response to a system call instruction, to selectively update each flag of a plurality of flags responsive to a corresponding indication in the mask" as recited in claim 1.

Still further, the Office Action alleges that the logical micro-op (add EAX, EBX, EAX) anticipates a system call instruction. Applicant respectfully disagrees. Hinton teaches "The logical micro-op, (add EAX, EBX, EAX), specifies adding the contents located in the logical register EAX with the contents located in the logical register EBX, and storing the result in the logical register EAX." (Hinton, col. 30, lines 23-27). This does not teach a system call instruction. Applicant respectfully submits that a system call instruction has a well known meaning in the art. Furthermore, a system call instruction is defined in the specification: "Generally, a system call instruction is an instruction defined for use in calling a more privileged code sequence." (Specification, page 19, lines 10-11). Hinton's add micro-op does not anticipate a system call instruction.

For at least the above stated reasons, Applicant submits that claim 1 is patentable over the cited art. Claims 2-8, being dependent from claim 1, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 2-8 recite additional combinations of features not taught or suggested in the cited art.

Claim 9 recites a combination of features including: "the processor is configured, in response to a system call instruction, to selectively update each flag of a plurality of

flags responsive to a corresponding indication in the mask". The teachings of Hinton, highlighted above, also fail to teach or suggest the above highlighted features of claim 9. Thus, claim 9 is patentable over the cited art. Claims 10-16, being dependent from claim 9, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 10-16 recite additional combinations of features not taught or suggested in the cited art.

Claim 17 recites a combination of features including: "processing a system call instruction, the processing including selectively updating each flag of a plurality of flags responsive to a corresponding indication in a mask". The teachings of Hinton, highlighted above, also fail to teach or suggest the above highlighted features of claim 17. Thus, claim 17 is patentable over the cited art. Claims 18-21, being dependent from claim 17, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 18-21 recite additional combinations of features not taught or suggested in the cited art.

Claim 22 recites a combination of features including: "the execution core is configured, in response to a system call instruction, to selectively update each flag of a plurality of flags responsive to the value in the register". The teachings of Hinton, highlighted above, also fail to teach or suggest the above highlighted features of claim 22. Thus, claim 22 is patentable over the cited art. Claims 23-27, being dependent from claim 22, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 23-27 recite additional combinations of features not taught or suggested in the cited art.

New Claims 28-39

Each of new claims 28-39 recites a combination of features not taught or suggested in the cited art. For example, claim 28 recites a combination of features including: "the processor is configured, in response to a system call instruction, to selectively update each flag of a plurality of flags responsive to the value in the storage location". Claims 29-33 depend from claim 28. Claim 34 recites a combination of

features including: "a plurality of instructions which, when executed in response to a system call instruction, selectively update each flag of a plurality of flags responsive to a value in a storage location". Claims 35-39 depend from claim 34.

Drawing Objection

The Office Action objected to the drawings, requesting that "SS" being included in the segment registers 1054 in Figs 12-14. Applicant files herewith replacement drawing sheets for Figs. 12-14 making the requested change. Accordingly, Applicant submits that the objection is addressed.

CONCLUSION

Applicant submits that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-78200/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☒ Please debit the above deposit account in the amount of $658 for fees ($180 IDS fee, $172 for 2 excess independent claims, and $306 for 17 claims over 20).

☒ Other: Three sheets of replacement drawings (Figs. 12-14), IDS including PTO-1449 form and cited references.

Respectfully submitted,

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